

ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit includes an input circuit which is provided with a reference potential conversion circuit. The reference potential conversion circuit is supplied with an external reference potential REF and outputs an internal reference potential VREFint differing from the external reference potential. The input circuit is supplied with an output potential VREFint from the reference potential conversion circuit as a reference potential REF. A data signal is also inputted to the input circuit. The input data signal is compared to the reference potential REF for generating a determination result. These operations improve the setup and hold times and enhance the voltage margin at the data acquisition time.